Graphene Field Effect Transistors with optimized Contact Resistance for Current Gain

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Introduction

Graphene is a promising two dimensional channel material for radio frequency field effect transistors (RF-FET)[1]. It has ambipolar carriers with high mobility and high saturation velocity. It also has excellent mechanical robustness and flexibility. Due to these intrinsic properties, graphene based FETs can be applied to flexible, wearable components for RF applications such as high speed wireless communication. GFETs fabricated on rigid and flexible substrate have been demonstrated by several groups [2-4]. Nevertheless, the high metal-to-graphene contact resistance remains a bottleneck factor for RF performance. i.e, current gain cut-off frequency, ft. In this work, we report a process and full characterization of GFETs based on CVD graphene on Si/SiO_2 substrate. A low contact resistance (Rc) of 125 ohm·µm with high reliability was obtained by using pure Au. From the measurement of scattering parameters, we extracted the high frequency performances of our GFETs. Best intrinsic transit frequency have been observed for transistor with 180 nm channel length, with intrinsic ft of 100 GHz at low bias of 0.5V.

Experimental Process

The device fabrication started by patterning bottom-gates (Al in 40nm thickness) on rigid silicon wafer by e-beam lithography and lift-off process. A thin layer of dielectric, Al_2O_3, was formed by natural oxidation of aluminum. After, the monolayer graphene was transferred on top of these pre-patterned bottom gates. The CVD grown graphene on copper foil associated with a wet transfer process was used. RIE O_2 plasma etching was used to define the graphene channel. Cr/Au 5/50 nm was first deposited on top of graphene channel for better adhesion and then the metal/graphene contacts were defined by using pure gold (30 nm thick). These Au-graphene contacts also define the drain to source distance, which is 400 nm. We complete the device fabrication process by defining the coplanar wave guide (CPW) access with deposition of Ni/Au 50/300 nm. The sketch of our GFETs is shown in Fig.1.

Results

We fabricated TLM structures together with other GFETs on the same chip. The electrical contacts are the same as for our GFETs. The resistance for different spacing, as shown in Fig.2.(a), were measured from 4 TLM devices. The resistance for the same electrode spacing is highly reproducible from the 4 TLM devices (deviation less than 10 percent). It indicates the good homogeneity of our contacts and graphene quality. In Fig.2 (b) we plot the resistance (average value from 4 TLM devices) versus contacts spacing. The red line is a linear fit to the data. The extracted Rc is 125 ohm·µm, one of the lowest value reported in literature for GFETs[2][3][5]. For transistor characterization, we performed at room temperature the DC and RF measurements by using Agilent DC parametric Analyzer and a Network Analyzer(Agilent E8361A), respectively. Fig.3 (a) shows the drain-to-source current as function of drain voltage with varying gate voltage. At drain voltage of 0.5V, the drain current varies from 10.8 mA to 24 mA. Fig.3 (c) shows the high frequency characterization which was carried out by measuring S-parameters from 0.1 to 50 GHz. Calibration procedure of line-reflect-reflect-match was performed prior to measurement so that the reference plane starts from CPW pads, as illustrated in Fig.3 (b) bottom image. The transit frequency obtained from the as-measured data account to the CPW access, we find for our best device f_t = 35 GHz. A de-embedding procedure is also implemented to extract the intrinsic performance. Open structure (same geometry to transistor but without graphene) was used to remove all the parasitic contribution from the CPW, a method as described in [6]. Moreover, the contact resistance contribution was removed by using the value extracted from TLM measurements. With this full de-embedding procedure, we report an intrinsic transit frequency of 100 GHz at a low bias of 0.5V.

Conclusion

We present GFETs based on low contact resistance of 125 ohm·µm. High current gain was obtained with extrinsic f_t of 35 GHz and an intrinsic f_t of 100 GHz for device with 180 channel length and 12 µm channel width. The high RF performance together with our bottom-gate structure (graphene is on top and exposed to ambient), provide an opportunity for applications such as optoelectronic components and high frequency sensors.

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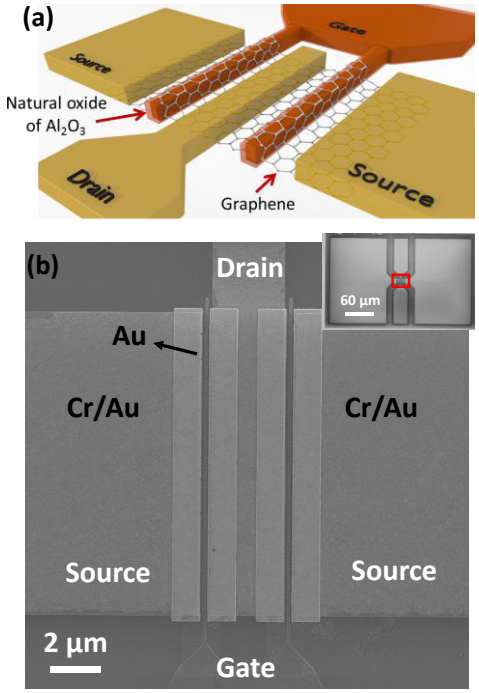

Fig. 1. Device structure with double bottom gates and natural oxide of aluminum. (a) GFET 3-D illustration. (b) SEM image of the transistor with double gates which are covered by graphene. The inset shows the transistor (marked by red rectangle) with CPW access.

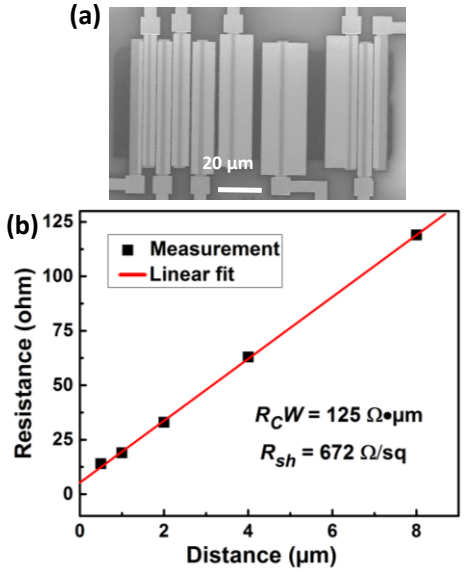

Fig. 2. Contact resistance. (a) SEM image of TLM structure. The width of contact is 48 µm and the contact spacing is 0.5, 1, 2, 4 and 8 µm. (b) Two point resistance versus contacts distance. The red line is the linear fitting of the measured data.

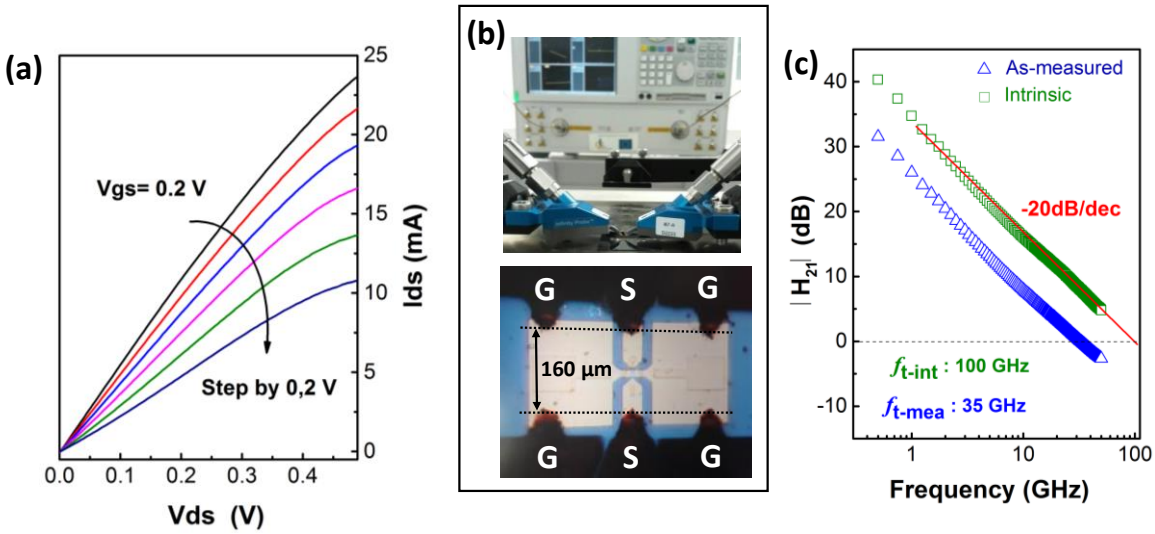

Fig. 3. Electrical characterization for GFET with channel length of 180 nm and channel width of 12µm. (a) Ids-Vds characteristics correspond to different gate voltage Vgs which varies from 0.2 V to 1.2 V. (b) Top: Measurement platform for both DC and RF measurements. Bottom: GSG infinity probes on CPW access with GFET in the center. The two dashed lines with 160 µm spacing illustrates the reference plane for S-parameters measurement. (c) The as-measured and intrinsic current gain, h21, as function of frequency at drain voltage of 0.5V. The as-measured results are without de-embedding, associating to the measurement plane of CPW pad as illustrated in (c) bottom. The intrinsic current gain was deduced after de-embedding.

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